. .'eescale Semiconductor
Technical Data

Document Number: MMA20312B
Rev. 2, 9/2014

RoHS

Heterojunction Bipolar Transistor Technology (InGaP HBT)

High Efficiency/Linearity Amplifier

MMA20312BT1

1800–2200 MHz, 27.2 dB
30.5 dBm
InGaP HBT LINEAR AMPLIFIER



QFN 3 × 3

The MMA20312B is a 2–stage high efficiency, Class AB InGaP HBT amplifier designed for use as a linear driver amplifier in wireless base station applications as well as an output stage in femtocell or repeater applications. It is suitable for applications with frequencies from 1800 to 2200 MHz such as TD–SCDMA, PCS, UMTS and LTE. The amplifier is housed in a cost–effective, surface mount QFN plastic package.

- Typical Performance: V_{CC} = 5 Vdc, I_{CQ} = 70 mA, P_{out} = 17 dBm

Frequency	G_{ps} (dB)	ACPR (dBc)	PAE (%)	Test Signal
1880 MHz	29.0	–47.4	9.1	TD–SCDMA
1920 MHz	29.0	–46.7	9.0	TD–SCDMA
2010 MHz	27.4	–52.0	9.3	TD–SCDMA
2025 MHz	26.8	–50.0	9.5	TD–SCDMA
2140 MHz	27.0	–51.7	9.4	W–CDMA

Features

- Frequency: 1800–2200 MHz
- P1dB: 30.5 dBm @ 2140 MHz (CW Application Circuit)
- Power Gain: 26.4 dB @ 2140 MHz (CW Application Circuit)
- OIP3: 44.5 dBm @ 2140 MHz (W–CDMA Application Circuit)
- Active Bias Control (adjustable externally)
- Single 5 V Supply
- Cost–effective 12–pin, 3 mm QFN Surface Mount Plastic Package
- In Tape and Reel. T1 Suffix = 1,000 Units, 12 mm Tape Width, 7–inch Reel.

Table 1. Typical CW Performance (1)

Characteristic	Symbol	1800 MHz	2140 MHz	2200 MHz	Unit
Small–Signal Gain (S21)	G_p	28.8	26.4	25.5	dB
Input Return Loss (S11)	IRL	–17.6	–10.9	–9.7	dB
Output Return Loss (S22)	ORL	–20.3	–14.7	–13.7	dB
Power Output @ 1dB Compression	P1dB	30.5	30.5	30.5	dBm

1. V_{CC1} = V_{CC2} = V_{BIAS} = 5 Vdc, T_A = 25°C, 50 ohm system, CW Application Circuit

Table 2. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	6	V
Supply Current	I_{CC}	550	mA
RF Input Power	P_{in}	14	dBm
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	175	°C

Table 3. Thermal Characteristics

Characteristic	Symbol	Value (2)	Unit
Thermal Resistance, Junction to Case Case Temperature 86°C, V_{CC1} = V_{CC2} = V_{BIAS} = 5 Vdc	$R_{\theta JC}$	52	°C/W

2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1955.

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Table 4. Electrical Characteristics (V_{CC1} = V_{CC2} = V_{BIAS} = 5 Vdc, 2140 MHz, T_A = 25°C, 50 ohm system, in Freescale W-CDMA Application Circuit)

Characteristic	Symbol	Min	Typ	Max	Unit
Small-Signal Gain (S21) (1)	G_p	23.6	27.2	—	dB
Input Return Loss (S11)	IRL	—	-10.7	—	dB
Output Return Loss (S22)	ORL	—	-15.5	—	dB
Power Output @ 1dB Compression, CW	P1dB	—	28.2	—	dBm
Third Order Output Intercept Point, Two-Tone CW	OIP3	—	44.5	—	dBm
Noise Figure	NF	—	3.3	—	dB
Supply Current (1)	I_{CQ}	62.5	70	77	mA
Supply Voltage	V_{CC}	—	5	—	V

Table 5. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	0, rated to 150 V
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	III

Table 6. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

1. Specified data is based on performance of soldered down part in W-CDMA application circuit.

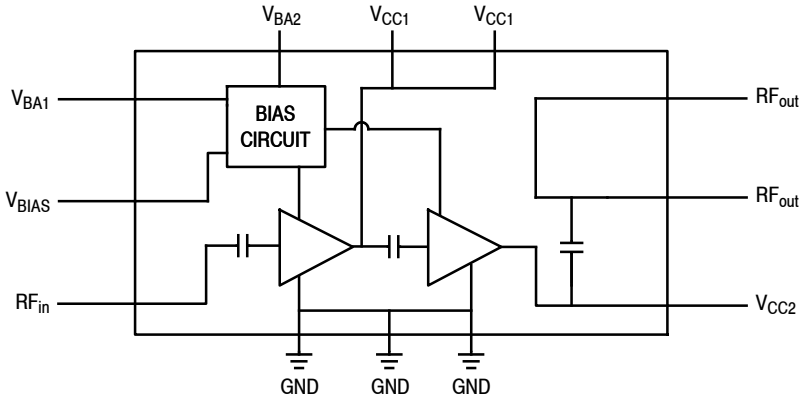


Figure 1. Functional Block Diagram

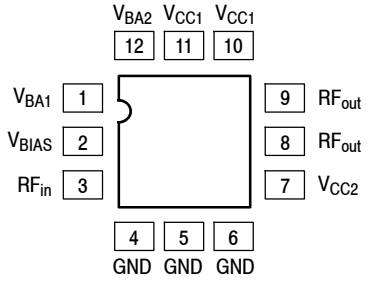
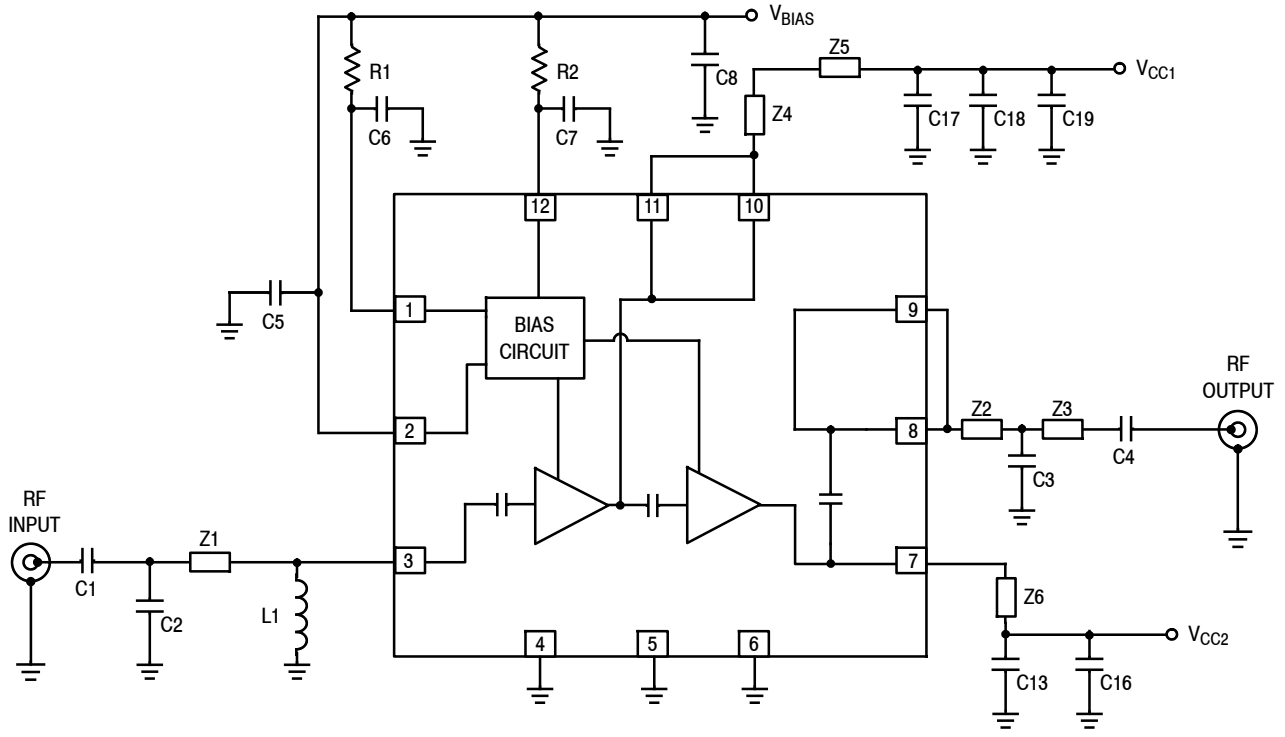


Figure 2. Pin Connections



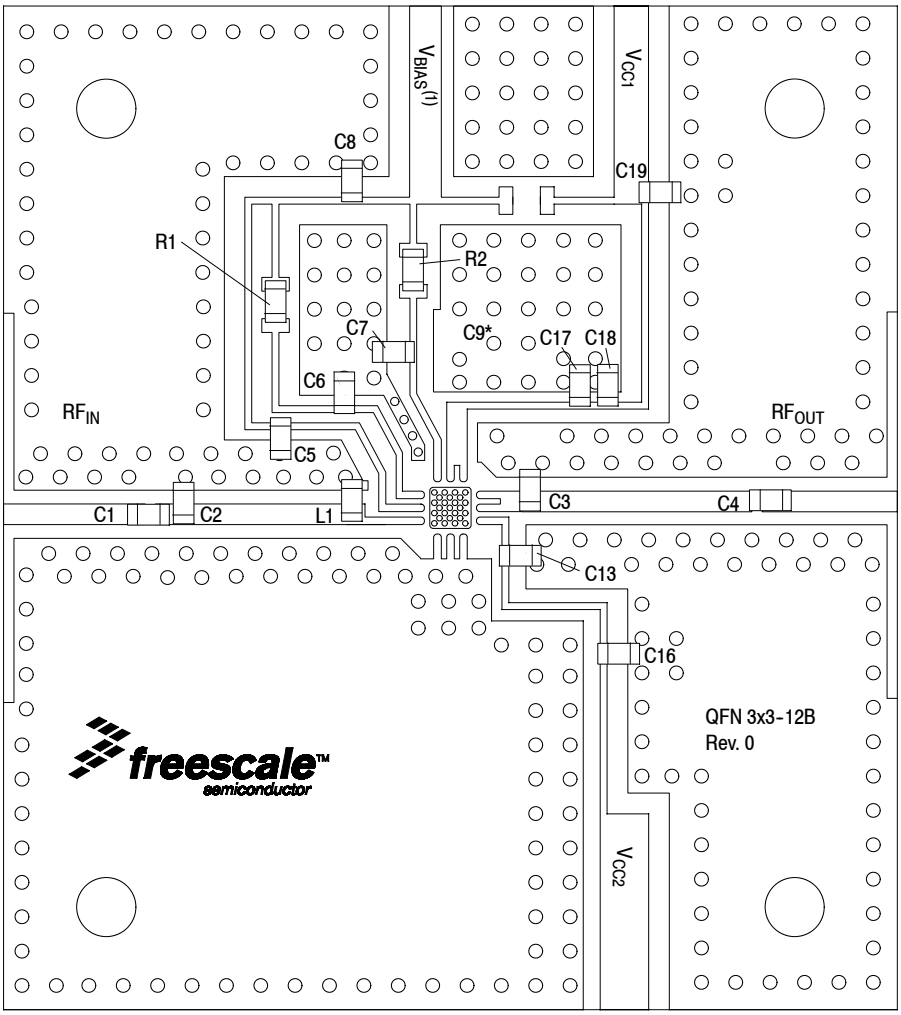
Z1	0.250″ x 0.030″ Microstrip	Z4	0.080″ x 0.030″ Microstrip
Z2	0.035″ x 0.030″ Microstrip	Z5	0.155″ x 0.010″ Microstrip
Z3	0.283″ x 0.030″ Microstrip	Z6	0.045″ x 0.010″ Microstrip

Figure 3. MMA20312BT1 Test Circuit Schematic — TD-SCDMA

Table 7. MMA20312BT1 Test Circuit Component Designations and Values — TD-SCDMA

Part	Description	Part Number	Manufacturer
C1, C5	22 pF Chip Capacitors	06033J220GBS	AVX
C2	1.8 pF Chip Capacitor	06035J1R8BBS	AVX
C3	2.2 pF Chip Capacitor	06035J2R2BBS	AVX
C4	5.6 pF Chip Capacitor	06035J5R6BBS	AVX
C6, C7, C13	10 pF Chip Capacitors	06035J100GBS	AVX
C8, C18	1 μF Chip Capacitors	GRM188R61A105KA61	Murata
C9	Component Not Placed		
C16, C19	10 μF Chip Capacitors	GRM188R60J106ME47	Murata
C17	0.1 μF Chip Capacitor	GRM188R71H104KA93	Murata
L1	1.8 nH Chip Inductor	LL1608-FS1N8S	TOKO
R1	120 Ω Chip Resistor	RR0816Q-121-D	Susumu
R2	1300 Ω Chip Resistor	RR0816Q-132-D	Susumu
PCB	0.01″, ε_r = 3.38	680-338	Isola

Note: Component number C9 is labeled on board but not placed. C10, C11, C12, C14 and C15 are intentionally omitted.



(1) V_{BIAS} [Board] supplies V_{BA1}, V_{BA2} and V_{BIAS} [Device].
Note: Component number C9* is labeled on board but not placed.

Figure 4. MMA20312BT1 Test Circuit Component Layout — TD-SCDMA

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C4	5.6 pF Chip Capacitor	06035J5R6BBS	AVX
C6, C7, C13	10 pF Chip Capacitors	06035J100GBS	AVX
C8, C18	1 μF Chip Capacitors	GRM188R61A105KA61	Murata
C9	Component Not Placed		
C16, C19	10 μF Chip Capacitors	GRM188R60J106ME47	Murata
C17	0.1 μF Chip Capacitor	GRM188R71H104KA93	Murata
L1	1.8 nH Chip Inductor	LL1608-FS1N8S	TOKO
R1	120 Ω Chip Resistor	RR0816Q-121-D	Susumu
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PCB	0.01″, ε_r = 3.38	680-338	Isola

Note: Component numbers C10, C11, C12, C14 and C15 are intentionally omitted.

(Test Circuit Component Designations and Values table repeated for reference.)

TYPICAL CHARACTERISTICS — TD-SCDMA

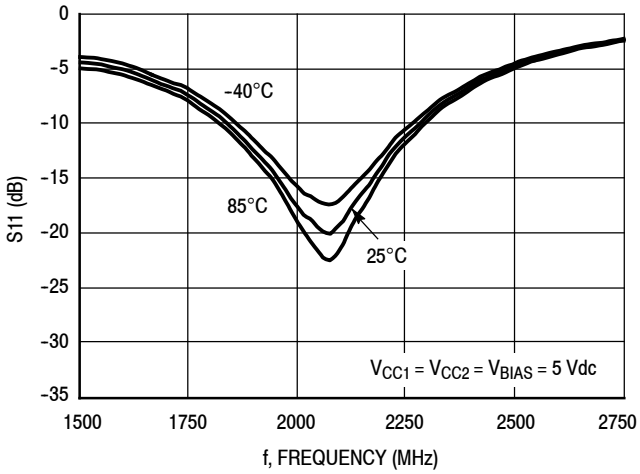


Figure 5. S11 versus Frequency versus Temperature

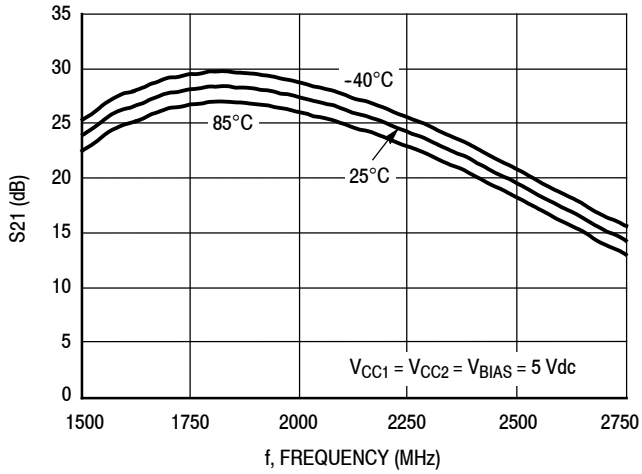


Figure 6. S21 versus Frequency versus Temperature

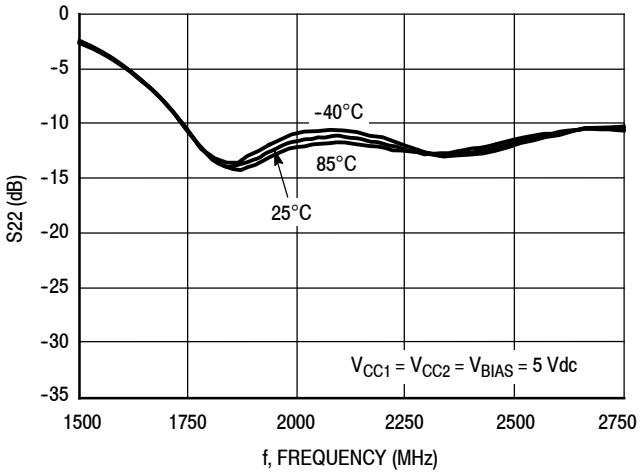


Figure 7. S22 versus Frequency versus Temperature

TYPICAL CHARACTERISTICS — TD-SCDMA

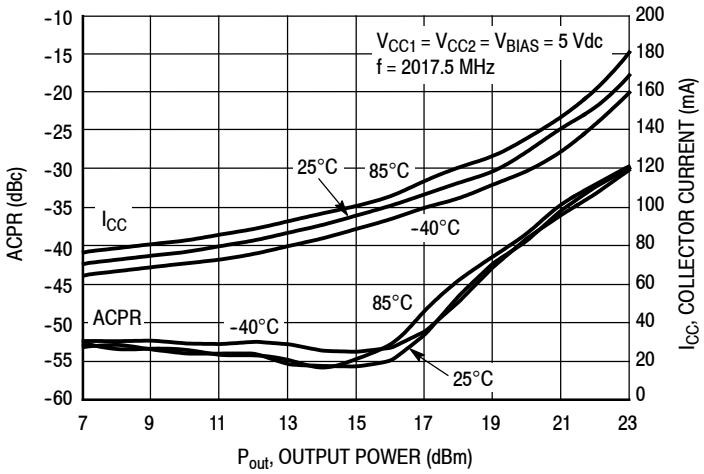


Figure 8. ACPR versus Collector Current versus Output Power versus Temperature

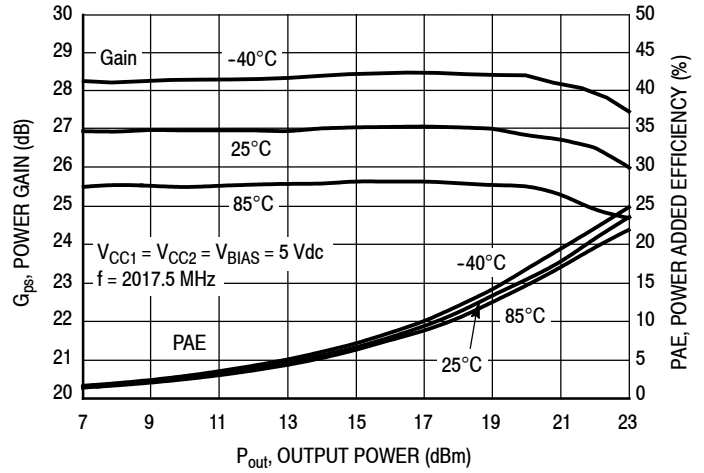


Figure 9. Power Gain versus Power Added Efficiency versus Output Power versus Temperature

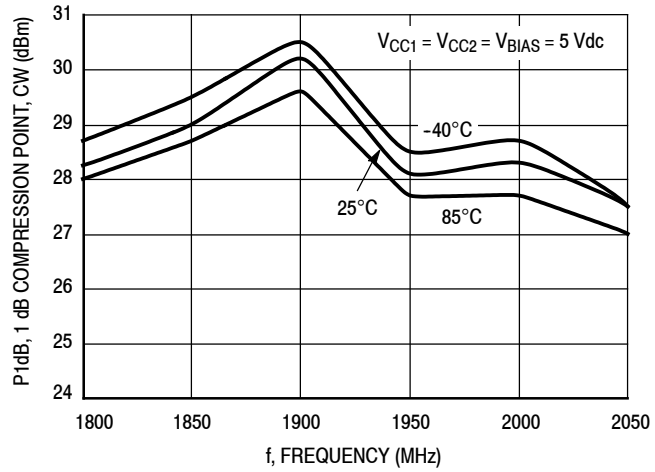
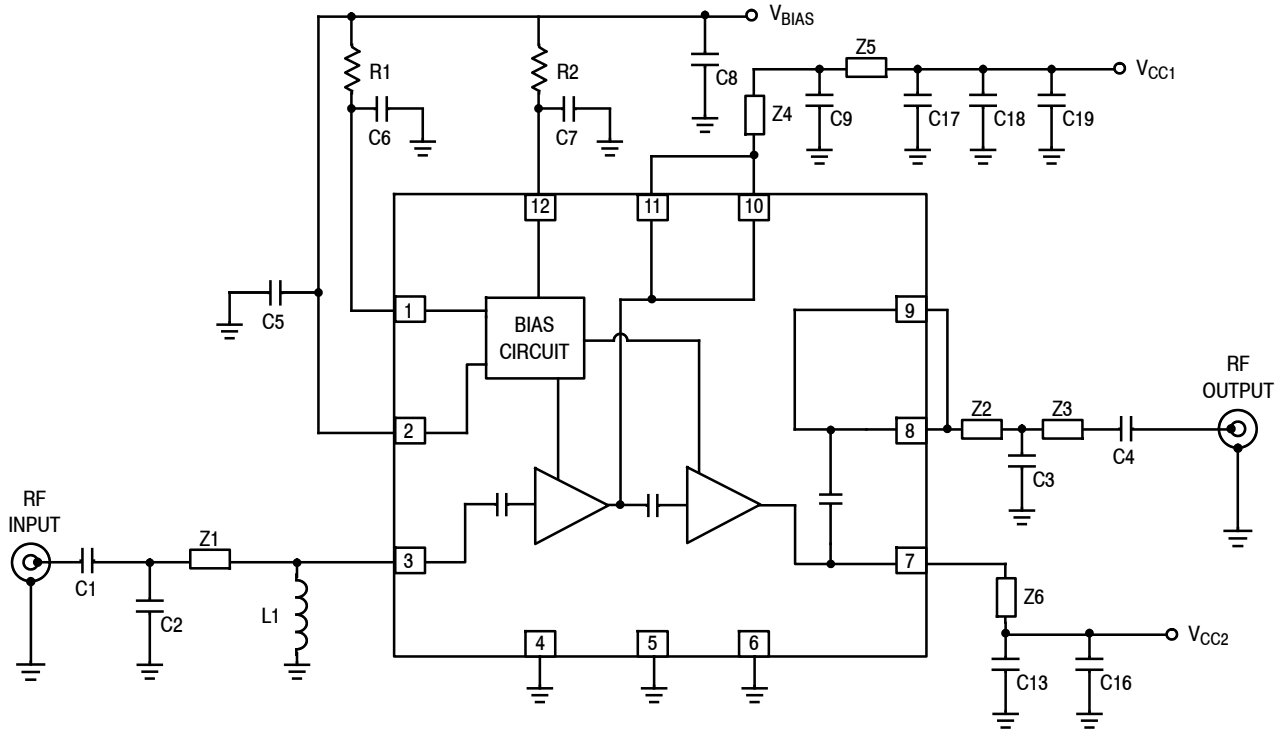


Figure 10. P1dB versus Frequency versus Temperature, CW



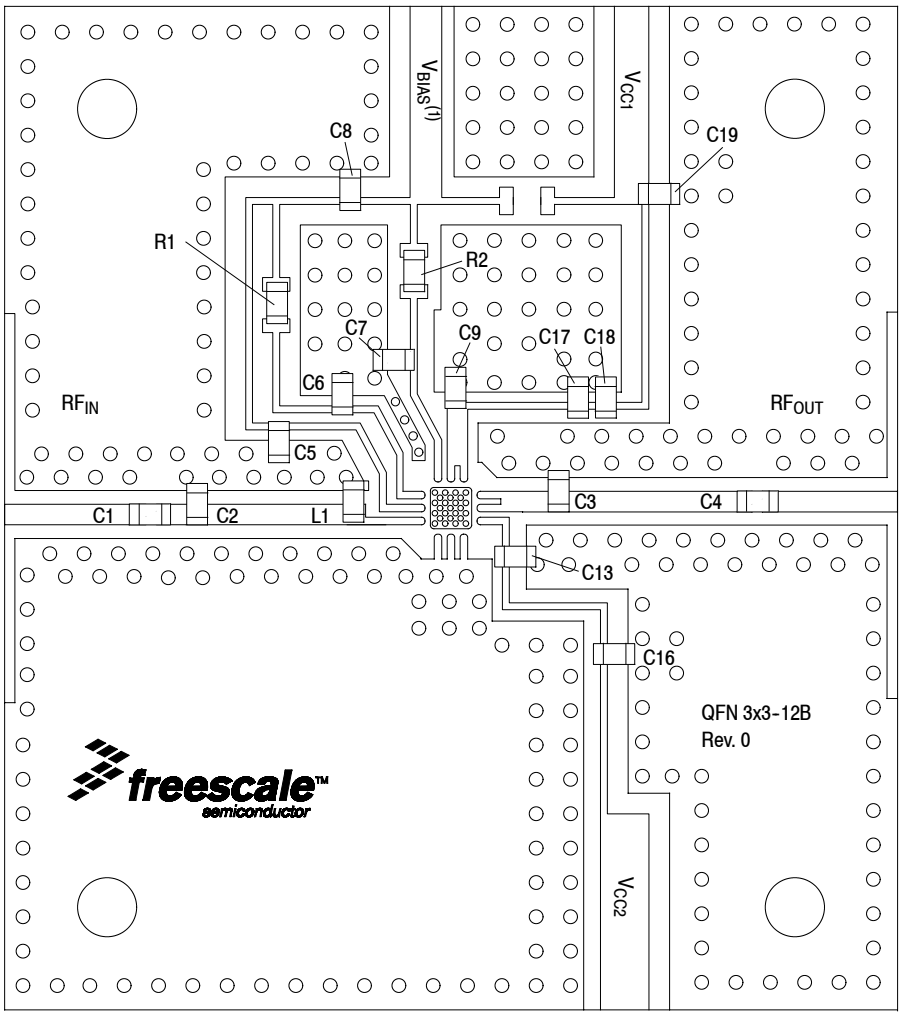
Z1	0.218″ x 0.030″ Microstrip	Z4	0.080″ x 0.030″ Microstrip
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Figure 11. MMA20312BT1 Test Circuit Schematic — W-CDMA

Table 8. MMA20312BT1 Test Circuit Component Designations and Values — W-CDMA

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C2, C3	1.8 pF Chip Capacitors	06035J1R8BBS	AVX
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C8, C18	1 μF Chip Capacitors	GRM188R61A105KA61	Murata
C16, C19	10 μF Chip Capacitors	GRM188R60J106ME47	Murata
C17	0.1 μF Chip Capacitor	GRM188R71H104KA93	Murata
L1	1.8 nH Chip Inductor	LL1608-FS1N8S	TOKO
R1	120 Ω Chip Resistor	RR0816Q-121-D	Susumu
R2	1500 Ω Chip Resistor	RR0816Q-152-D	Susumu
PCB	0.01″, ε_r = 3.38	680-338	Isola

Note: Component numbers C10, C11, C12, C14 and C15 are intentionally omitted.



(1) V_{BIAS} [Board] supplies V_{BA1}, V_{BA2} and V_{BIAS} [Device].

Figure 12. MMA20312BT1 Test Circuit Component Layout — W-CDMA

Table 8. MMA20312BT1 Test Circuit Component Designations and Values — W-CDMA

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L1	1.8 nH Chip Inductor	LL1608-FS1N8S	TOKO
R1	120 Ω Chip Resistor	RR0816Q-121-D	Susumu
R2	1500 Ω Chip Resistor	RR0816Q-152-D	Susumu
PCB	0.01″, ε_r = 3.38	680-338	Isola

Note: Component numbers C10, C11, C12, C14 and C15 are intentionally omitted.

(Test Circuit Component Designations and Values table repeated for reference.)

TYPICAL CHARACTERISTICS — W-CDMA

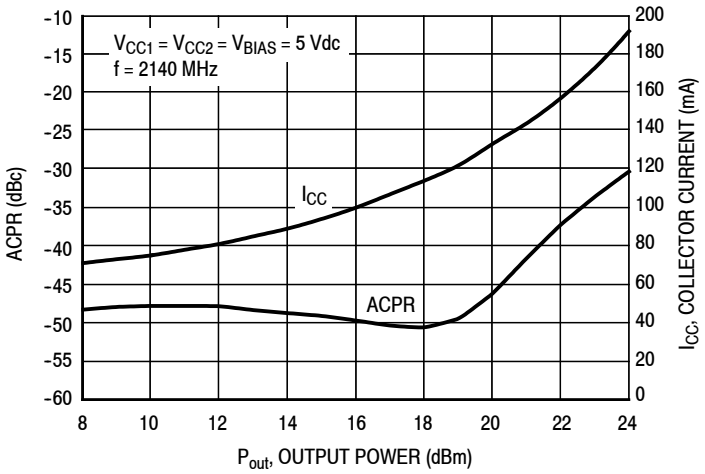


Figure 13. ACPR versus Collector Current versus Output Power

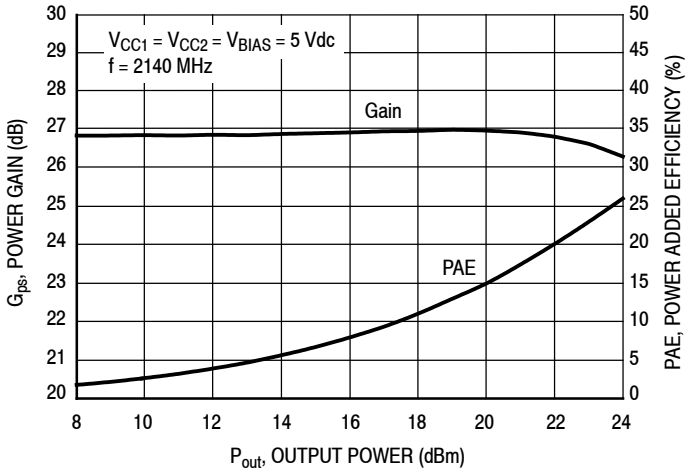


Figure 14. Power Gain versus Power Added Efficiency versus Output Power

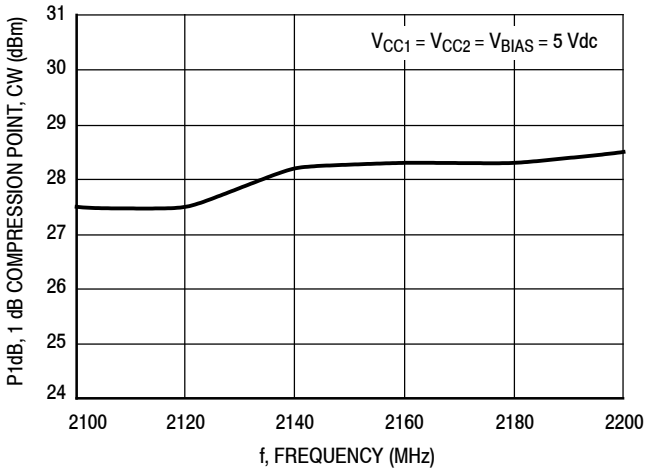


Figure 15. P1dB versus Frequency, CW

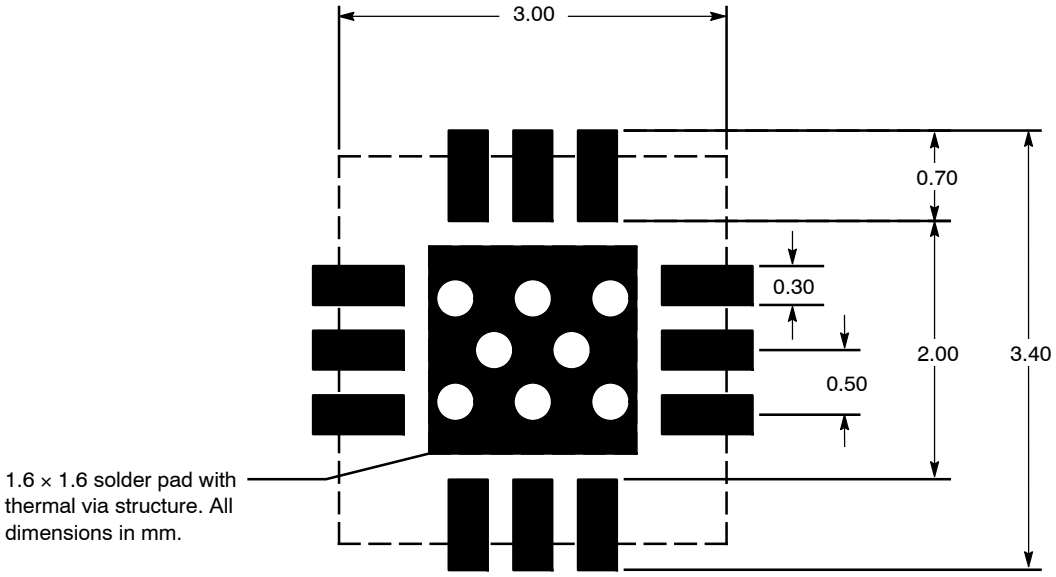
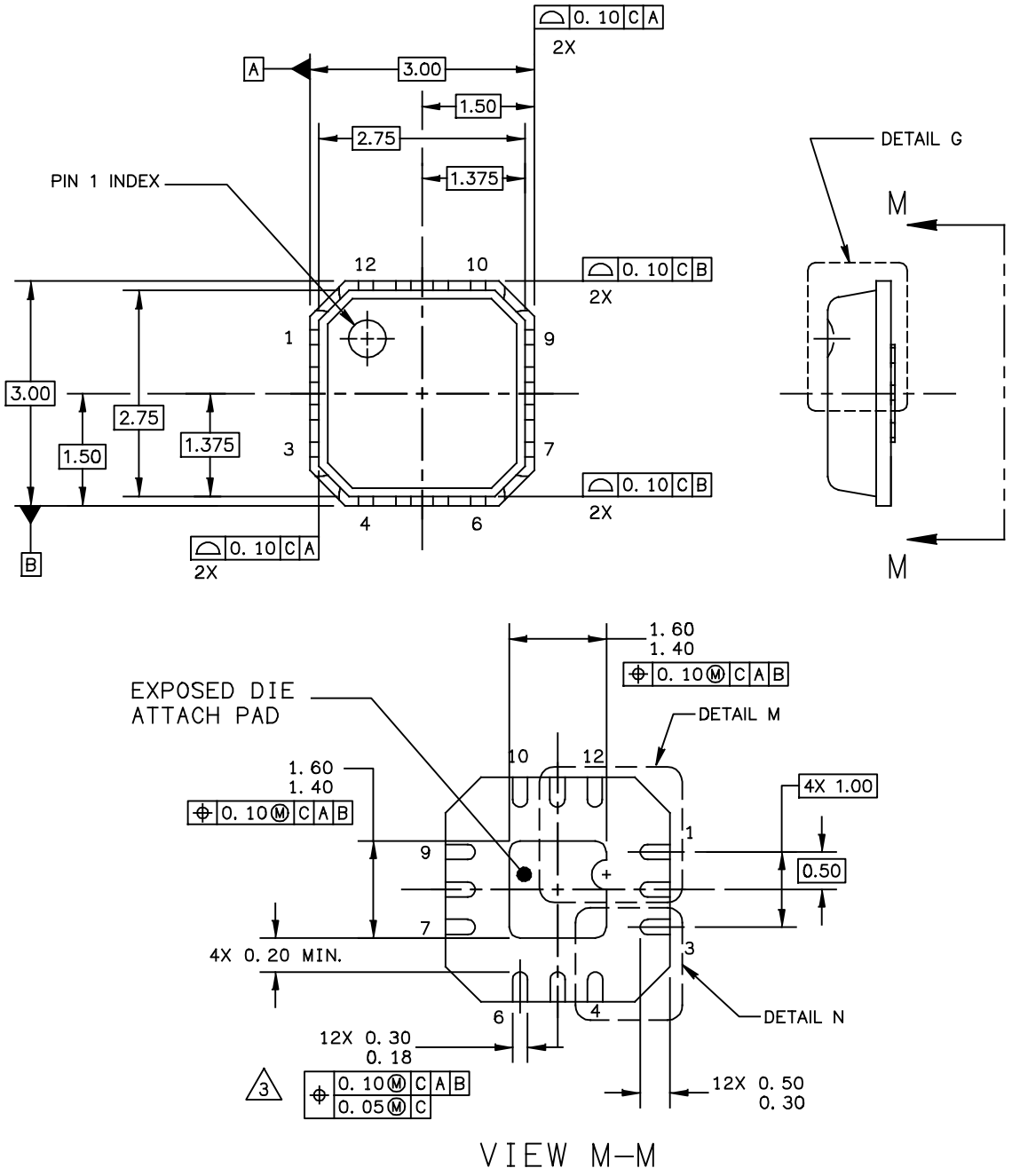


Figure 16. PCB Pad Layout for QFN 3 × 3

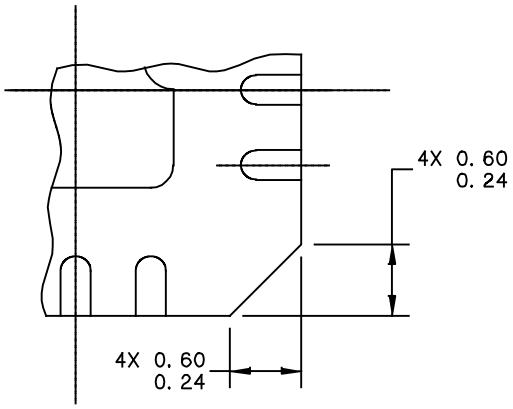


Figure 17. Product Marking

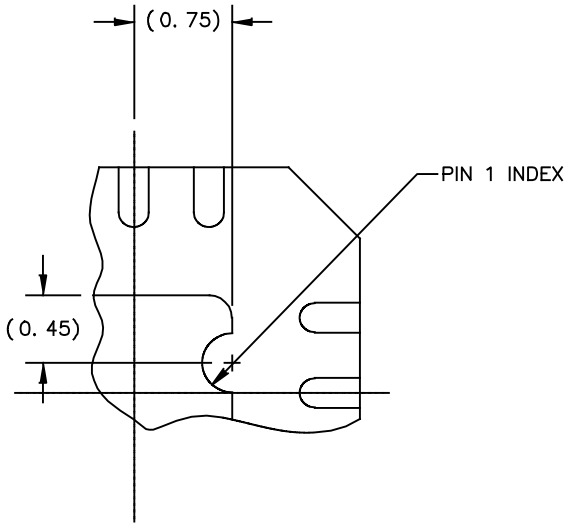
PACKAGE DIMENSIONS



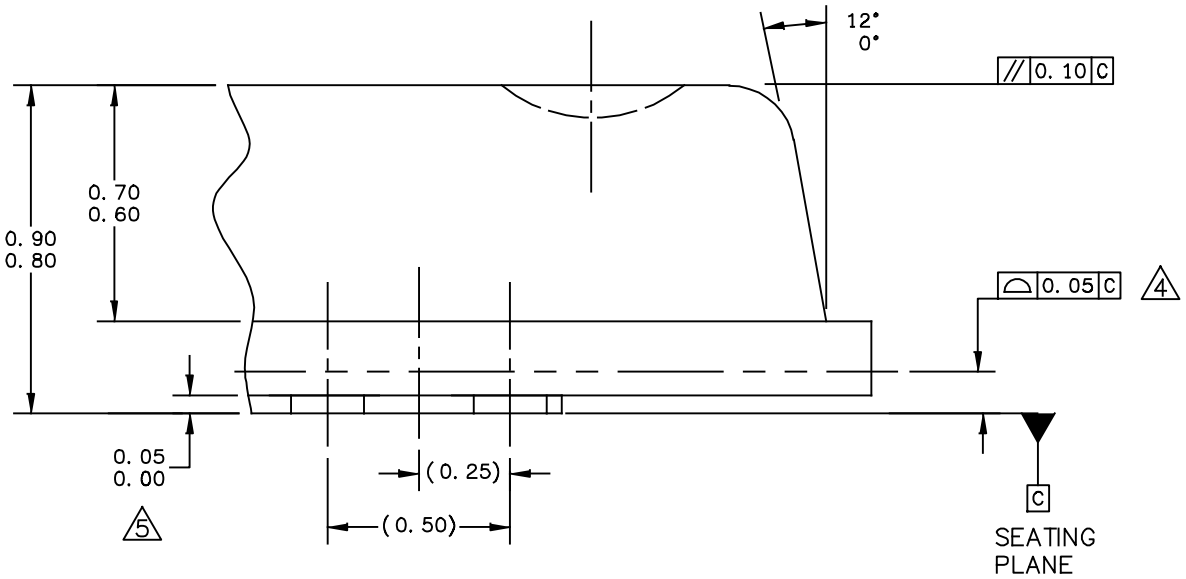
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TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 12 TERMINAL, 0.5 PITCH (3X3X0.85)	DOCUMENT NO: 98ASA00227D	REV: O
	CASE NUMBER: 2131–01	14 MAY 2010
	STANDARD: NON–JEDEC	



DETAIL N
CORNER CONFIGURATION



DETAIL M
PIN 1 BACKSIDE INDEX



DETAIL G
VIEW ROTATED 90° CW

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NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING & TOLERANCING PER ASME Y14.5 – 2009.

3. THIS DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.

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	STANDARD: NON–JEDEC	

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Software

- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to Software & Tools on the part’s Product Summary page to download the respective tool.

FAILURE ANALYSIS

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where Freescale is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local Freescale Sales Office.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Oct. 2010	• Initial Release of Data Sheet
1	Mar. 2011	• Added “OIP3: 44.5 dBm @ 2140 MHz (W-CDMA Application Circuit)” to Features list, p. 1 • Typical CW Performance table: removed OIP3, p. 1 • Figs. 4 and 12, Test Circuit Component Layout, updated component part layout identifier to reflect package type. Changed from MMA20312B to QFN 3x3-12B, pp. 4, 8
1.1	Mar. 2011	• Updated device descriptor box to reflect W-CDMA application circuit small-signal gain value, p. 1
1.2	Feb. 2012	• All references to “V_{CTRL}” in the data sheet tables, test circuit schematics and component layouts are replaced with “V_{BIAS}”. V_{BIAS} is the supply voltage which sets the internal bias conditions via pins 1, 2, and 12, p. 1-3, 5-7, 9. Footnote “(1) V_{BIAS} [Board] supplies V_{BA1}, V_{BA2} and V_{BIAS} [Device]” added to test circuit component layouts, pp. 4, 8. • Fig. 3, Test Circuit Schematic - TD-SCDMA, Table 7, Test Circuit Component Designations and Values - TD-SCDMA, Fig. 4, Test Circuit Component Layout - TD-SCDMA, Fig. 11, Test Circuit Schematic - W-CDMA, Table 8, Test Circuit Component Designations and Values - W-CDMA and Fig. 12, Test Circuit Component Layout - W-CDMA: clarified components not placed and components intentionally omitted, pp. 3, 4, 7, 8
2	Sept. 2014	• Table 2, Maximum Ratings: updated Junction Temperature from 150°C to 175°C to reflect recent test results of the device, p. 1 • Added Failure Analysis information, p. 14

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Rev. 2, 9/2014